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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,309	09/12/2005	Joon-Hoo Choi	ABS-1700 US	1450

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EXAMINER	
SALERNO, SARAH KATE	
ART UNIT	PAPER NUMBER
2814	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/521,309	CHOI ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-6 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment/arguments filed on 04/10/08 as being acknowledged and entered. By this amendment claims 7-9 & 14 are canceled, no new claims have been added claims 1-6 & 10-13 are pending and no claims are withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 6, 10 & 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US PGPub 2001/0026125) in view of Hwang et al. (US PGPub 2002/0158995).

Claim1: Yamazaki teaches an organic EL display panel comprising (FIG. 6): an insulating substrate (11); a polysilicon layer formed on the substrate (13-17, 31-32 & 34); a gate insulating layer (18) formed on the polysilicon layer (13-17, 31-32 & 34); a gate wire (611) formed on the gate insulating layer (18); an interlayer insulating film (20) formed on the gate wire; a data wire formed on the interlayer insulating film (20); an organic EL layer (43) formed on the pixel electrode (40) and disposed in a predetermined area; a partition (41a) formed on the data wire and the pixel electrode and defining the predetermined area; and a common electrode (44) formed on the organic EL layer (43) and the partition (41a). Yamazaki does not teach a pixel electrode

formed on the same layer as the data wire. Hwang teaches a pixel electrode formed on the same layer as the data wire to reduce processing steps [0022, 0026]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Yamazaki to teach the a pixel electrode formed on the same layer as the data wire to reduce processing steps as taught by Hwang [0022, 0026].

Claim 2: Hwang teaches the pixel electrode includes the same material as the data wire [0022, 0026].

Claims 3 & 10: Yamazaki teaches the polysilicon layer (13-17, 31-32 & 34) comprises first (601) and second transistor portions (602) including source regions (13, 36) and drain regions (14 & 32) and a storage electrode portion (51) connected to the second transistor portion (602), the gate wire comprises first (19a) and second (35) gate electrodes and a storage electrode (35) overlapping the first (601) and the second transistor (602) portions and the storage electrode portion (51), respectively, the data wire comprises first and second data lines, a first source electrode (21) connected to the first data line and the source region (13) of the first transistor portion (601), a first drain electrode (22) connected to the drain region (14) the first transistor portion (601) and the second gate electrode (35), and a second source electrode (36) connected to the second data line and the source region (31) of the second transistor portion (602), and the pixel electrode (40) is connected to the drain region (32) of the second transistor (602) (FIG. 6, 7A; [0078-0091].

Claims 6 & 13: Yamazaki teaches an auxiliary electrode (41b) contacting the common electrode (44) (FIG. 6).

4. Claims 4 & 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US PGPub 2001/0026125) in view of Hwang et al. (US PGPub 2002/0158995) as applied to claims 1 & 2 above, and further in view of Aoki et al. (US PGPub 2001/0022497).

Regarding claims 4 & 11, as described above, Yamazaki and Hwang substantially read on the invention as claimed, except Yamazaki and Hwang do not teach a buffer layer disposed between the organic EL layer and the common electrode. Aoki teaches a layer between the EL layer and the cathode to improve electron injection properties of the EL device [0098]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Yamazaki and Hwang to contain a buffer layer between the El layer and the cathode to improve electron injection properties of the EL device as taught by Aoki [0098].

5. Claims 5 & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (US PGPub 2001/0026125) in view of Hwang et al. (US PGPub 2002/0158995) as applied to claims 1 & 2 above, and further in view of Yamazaki et al. (US Patent 6,013,930).

Regarding claims 5 & 12, as described above, Yamazaki and Hwang substantially read on the invention as claimed, and Yamazaki ('995) teaches the partitions being made of an acrylic resin film but not of black photoresist. Yamazaki

('930) teaches the use of a black photosensitive acrylic resin between pixel electrodes (Col. 25 lines 30-67) to produce a highly-reliable and highly reproducible device (col. 2 lines 23-30). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Yamazaki ('995) and Hwang to make the acrylic resin a black photosensitive acrylic resin to produce a highly-reliable and highly reproducible device as taught by ('930) (col. 2 lines 23-30).

Response to Arguments

6. Applicant's arguments filed 04/01/08 have been fully considered but they are not persuasive.

Applicant argues that Yamazaki and Hwang do not teach "a partition formed on the data wire..." Applicant's arguments are not persuasive because Yamazaki teaches a partition (41a) on the data wire (36) and the pixel electrode (40) as seen in figure 6.

Applicant argues that Yamazaki ('930) does not teach "the partition comprises black photoresist" because the black matrices taught by '930 do not correspond to the partitions of claim 1. As stated in the previous office action and above, '930 was not used to teach the partitions defining an area on which an EL layer is to be formed as required by claim 1, Yamazaki '125 was used to teach the partitions defining an area on which an EL layer is to be formed as required by claim 1.

Applicant argues that there is no motivation to combine Yamazaki and Hwang. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, there is motivation to combine Hwang with Yamazaki ('125) because Hwang's device forms the pixel electrode and date wire on the same layer to reduce the number of steps needed to make the TFT part of the display device which is common to both Yamazaki ('125) and Hwang.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-F 8:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. K. S./
Examiner, Art Unit 2814

/Theresa T. Doan/
Primary Examiner, Art Unit 2814